LMX2542 PLLatinum™ Cellular and GPS Frequency Synthesizer System with Integrated VCO

Check for Samples: LMX2542

FEATURES

- **Small Size**
  - **5.0 mm x 5.0 mm x 0.75 mm 28-Pin WQFN**
- **RF Synthesizer System**
  - **Integrated RF VCO**
  - **Integrated Loop Filter**
  - **Low Spurious, Low Phase Noise Fractional-N RF PLL Based on 11-Bit ΔΣ Modulator**
  - **5 kHz Frequency Resolution**
  - **Cellular-CDMA LO: 2105.28 MHz to 2155.14 MHz (Requires an External LO /2 Circuit)**
  - **GPS LO: 2087.73 MHz**
  - **(Requires an External LO /1.5 Circuit)**
- **IF Synthesizer System**
  - **Integer-N IF PLL**
  - **Programmable Charge Pump Current Levels**
  - **IF LO: 367.20 MHz**
- **Supports Various Reference Oscillator Frequencies:**
  - **19.20 MHz/ 19.68 MHz**
- **Low Current Consumption:**
  - **22 mA Typical at 2.8V**
- **2.7V to 3.3V Operation**
- **RF Digital Filtered Lock Detect Output**
- **Hardware and Software Powerdown Control**

APPLICATIONS

- **Cellular-CDMA 1xRTT and IS-95 Mobile Handsets with GPS**
- **Cellular-CDMA 1xRTT and IS-95 Mobile Data Systems with GPS**

DESCRIPTION

LMX2542 is a highly integrated, high performance, low power frequency synthesizer system optimized for Cellular-CDMA 1xRTT and IS-95 mobile handsets and data systems with GPS capabilities. Using a proprietary digital phase locked loop technique, LMX2542 provides very stable, low noise local oscillator (LO) signals for up and down conversion in wireless communications devices.

LMX2542 includes a Voltage Controlled Oscillator (VCO) for both the Cellular-CDMA and GPS frequency bands, a loop filter, and a Fractional-N RF PLL based on a Delta Sigma (ΔΣ) modulator. In concert, these blocks form a closed loop RF synthesizer system. The RF synthesizer system operates from 2087.73 MHz to 2155.14 MHz.

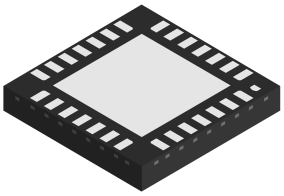
LMX2542 includes an Integer-N IF PLL also. For more flexible loop filter designs, the IF PLL includes a 4-level programmable charge pump. Together with an external VCO and loop filter, LMX2542 makes a complete closed loop IF synthesizer system. The default IF frequency is 367.20 MHz.

Serial data is transferred to the device via a three-wire MICROWIRE™ interface (DATA, LE, CLK).

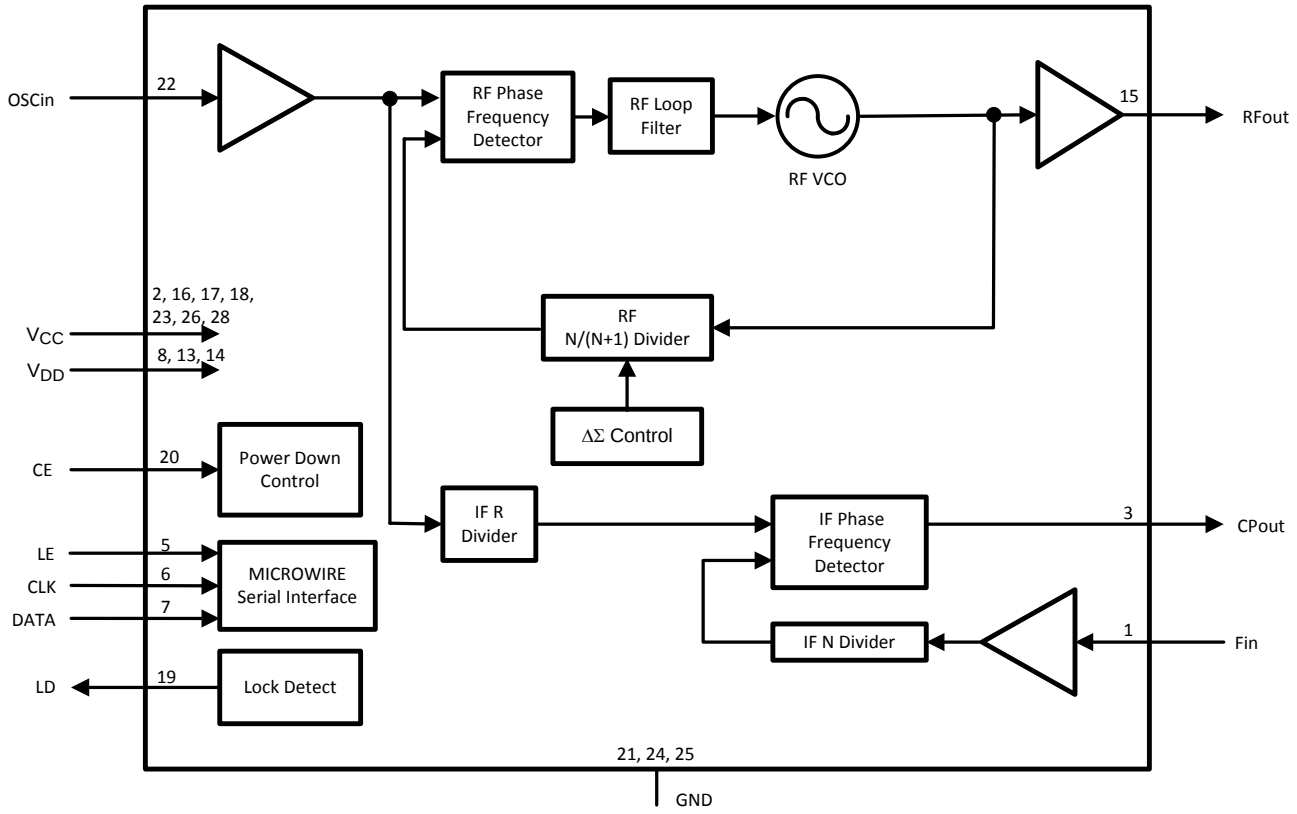
Operating supply voltage ranges from 2.7V to 3.3V. LMX2542 features low current consumption: 22 mA at 2.8V.

LMX2542 is available in a 28-Pin Leadless Leadframe Package (WQFN).

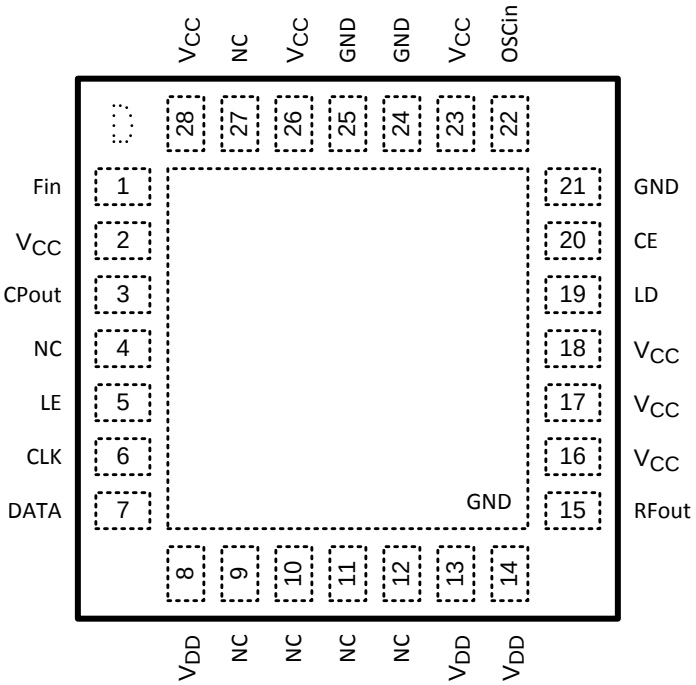
Leadless Leadframe Package



Functional Block Diagram



Connection Diagram



Note: Analog GND connected through exposed die attached pad.

Leadless Leadframe Package (WQFN)
(Top View)
See Package Number NJB

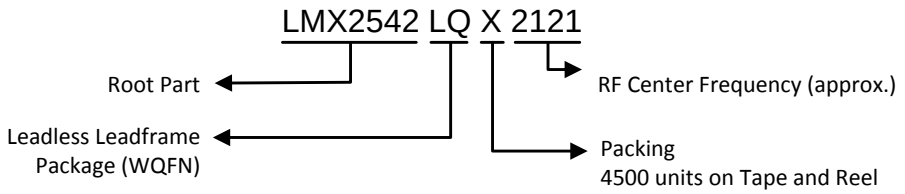
PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	Fin	I	IF PLL buffer/prescaler input. Small signal input from the VCO.
2	V_{CC}	—	Power supply bias for the IF PLL analog circuits. V_{CC} may range from 2.7V to 3.3V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane on the printed circuit board.
3	CPout	O	IF PLL charge pump output. The output is connected to the external loop filter, which drives the input of the IF VCO.
4	NC	—	No Connect. Do not connect to any node on the printed circuit board.
5	LE	I	MICROWIRE Latch Enable Input. High impedance CMOS input. When LE transitions from LOW to HIGH, DATA stored in the shift register is loaded into one of 6 internal control registers.
6	CLK	I	MICROWIRE Clock Input. High impedance CMOS input. DATA is clocked into the 24-bit shift register on the rising edge of CLK.
7	DATA	I	MICROWIRE Data Input. High impedance CMOS input. Binary serial data. The MSB of DATA is shifted in first.
8	V_{DD}	—	Power supply bias for the RF VCO. V_{DD} may range from 2.7V to 3.3V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane on the printed circuit board.
9	NC	—	No Connect. Do not connect to any node on the printed circuit board.
10	NC	—	No Connect. Do not connect to any node on the printed circuit board.
11	NC	—	No Connect. Do not connect to any node on the printed circuit board.
12	NC	—	No Connect. Do not connect to any node on the printed circuit board.

PIN DESCRIPTION (continued)

Pin No.	Pin Name	I/O	Description
13	V_{DD}	—	Power supply bias for the RF VCO. V_{DD} may range from 2.7V to 3.3V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane on the printed circuit board.
14	V_{DD}	—	Power supply bias for the RF VCO output buffer. V_{DD} may range from 2.7V to 3.3V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane on the printed circuit board.
15	RFout	O	Buffered RF VCO output.
16	V_{CC}	—	Power supply bias for the RF PLL prescaler. V_{CC} may range from 2.7V to 3.3V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane on the printed circuit board.
17	V_{CC}	—	Power supply bias for the RF PLL charge pump. V_{CC} may range from 2.7V to 3.3V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane on the printed circuit board.
18	V_{CC}	—	Power supply bias for the RF PLL digital circuits. V_{CC} may range from 2.7V to 3.3V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane on the printed circuit board.
19	LD	O	Digital filtered lock detect output.
20	CE	I	Chip Enable input. High Impedance CMOS input. When this pin is set HIGH, the RF and IF synthesizer systems are powered up. Powerdown is then controlled through the MICROWIRE. When this pin is set LOW, the device is asynchronously powered down and the IF PLL charge pump output is forced to a high impedance state (Tri-State).
21	GND	—	Ground for the RF PLL digital circuits.
22	OSCin	I	Reference oscillator input. The input is driven by an external AC coupled source. When the OSC_FREQ bit is set LOW, a 19.20 MHz reference frequency should be used. When the OSC_FREQ bit is set HIGH, a 19.68 MHz reference frequency should be used.
23	V_{CC}	—	Power supply bias for the reference oscillator buffer. V_{CC} may range from 2.7V to 3.3V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane on the printed circuit board.
24	GND	—	Ground for the reference oscillator buffer.
25	GND	—	Ground for the IF PLL digital circuits.
26	V_{CC}	—	Power supply bias for the IF PLL digital circuits. V_{CC} may range from 2.7V to 3.3V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane on the printed circuit board.
27	NC	—	No Connect. Do not connect to any node on the printed circuit board.
28	V_{CC}	—	Power supply bias for the IF PLL buffer/ prescaler. V_{CC} may range from 2.7V to 3.3V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane on the printed circuit board.

Part Number Description



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)(4)

Power Supply Voltage	V_{CC} to GND	−0.3V to +3.6V
	V_{DD} to GND	−0.3V to +3.6V
Voltage on any pin to GND (V_{IN})	V_{IN} must be < +3.6V	−0.3V to V_{CC}+0.3V
		−0.3V to V_{DD}+0.3V
Storage Temperature Range (T_S)		−65°C to +150°C
Lead Temperature (solder 4 s) (T_L)		+260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, refer to the Electrical Characteristics section. The ensured specifications apply only for the conditions listed.
(2) This device is a high performance RF integrated circuit with an ESD rating < 2kV and is ESD sensitive. Handling and assembly of this device should be done at ESD protected work stations.
(3) GND = 0V.
(4) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

Power Supply Voltage	V_{CC} to GND	+2.7V to +3.3V
	V_{DD} to GND	+2.7V to +3.3V
Operating Temperature (T_A)		−30°C to +85°C

Electrical Characteristics

V_{CC} = V_{DD} = CE = 2.8V, T_A = +25°C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
Icc PARAMETERS						
I_{CC} + I_{DD}	Power Supply Current (RF and IF Synthesizer Systems)	RF_EN Bit = 1 IF_EN Bit = 1 OB_CRL[1:0] Word = 00 VCO_CUR[1:0] Word = 11 IF_CUR[1:0] Word = 00		22.0	24.0	mA
(I_{CC} + I_{DD})$_{RF}$	Power Supply Current (RF Synthesizer System)	RF_EN Bit = 1 IF_EN Bit = 0 OB_CRL[1:0] Word = 00 VCO_CUR[1:0] Word = 11		20.0	22.0	mA
I_{PD}	Powerdown Current	CE, CLK, DATA and LE = 0V OSCin = 0V (RF_EN Bit = 0 and IF_EN Bit = 0)			20.0	µA
RF SYNTHESIZER SYSTEM PARAMETERS						
RF VCO						
f_{RFout}	RF VCO Operating Frequency(1)(2)		2087.73		2155.14	MHz
p_{RFout}	RF VCO Output Power	OB_CRL[1:0] Word = 00	−7.5	−4.5	−1.5	dBm
		OB_CRL[1:0] Word = 01	−5.0	−2.0	1.0	dBm
		OB_CRL[1:0] Word = 10	−2.5	0.5	3.5	dBm
		OB_CRL[1:0] Word = 11	0.0	3.0	6.0	dBm
φ_{eRF}	RF VCO RMS Phase Error			1.3		Deg.
L_{RF}(f)	RF VCO Single Side Band Phase Noise	f = 100 kHz Offset TCXO Reference Source OSC_FREQ Bit = 0 or 1 OB_CRL[1:0] Word = 11 IF_EN Bit = 0		−109	−107	dBc/ Hz
		f = 900 kHz Offset TCXO Reference Source OSC_FREQ Bit = 0 or 1 OB_CRL[1:0] Word = 11 IF_EN Bit = 0		−134	–133	dBc/ Hz
$SPURS_{RF}$	RF Synthesizer Reference Spurs	OSC_FREQ Bit = 0 or 1 IF_EN Bit = 0			−75	dBc
HS_{RF}	RF VCO Harmonic Suppression	2^{ND} Harmonic OB_CRL[1:0] Word = 11			−25	dBc
		3^{RD} Harmonic OB_CRL[1:0] Word = 11			−25	dBc
t_{RFLOCK}	Channel Switch Lock Time(3)	$f_{INITIAL}$ = 2087.73 MHz f_{FINAL} = 2155.14 MHz		1.0	1.3	ms

(1) For other RF frequency ranges, please contact Texas Instruments.
(2) When the Cellular-CDMA mode is used, an external /2 circuit is required before the Cellular mixer LO port. Furthermore, if an external /1.5 circuit is available before the GPS mixer LO port, the GPS frequency of 1391.82 MHz can be achieved by using a fixed RF frequency of 2087.73 MHz.
(3) Lock time is defined as the time difference between the beginning of the frequency transition and the point at which the frequency remains within +/- 1 kHz of the final frequency. t_{LOCK}= t_{FINAL} − $t_{INITIAL}$.

Electrical Characteristics (continued)

V_{CC} = V_{DD} = CE = 2.8V, T_A = +25°C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
IF SYNTHESIZER SYSTEM PARAMETERS						
f_{Fin}	IF Synthesizer Operating Frequency(4)	SPI_DEF Bit = 1 IF_FREQ[1:0] Word = 00		170.76		MHz
		SPI_DEF Bit = 1 IF_FREQ[1:0] Word = 01 (Default)		367.20		MHz
		SPI_DEF Bit = 1 IF_FREQ[1:0] Word = 10		440.76		MHz
$f_{\varphi IF}$	IF Synthesizer Phase Detector Frequency			120		kHz
p_{Fin}	IF Synthesizer Input Sensitivity		-12		0	dBm
$I_{CPoutIF}$	IF Synthesizer Charge Pump Output Current	IF_CUR[1:0] Word = 00		100		µA
		IF_CUR[1:0] Word = 01		200		µA
		IF_CUR[1:0] Word = 10		300		µA
		IF_CUR[1:0] Word = 11		800		µA
REFERENCE OSCILLATOR PARAMETERS						
f_{OSCin}	Reference Oscillator Input Operating Frequency(5)	OSC_FREQ Bit = 0	19.20			MHz
		OSC_FREQ Bit = 1			19.68	MHz
v_{OSCin}	Reference Oscillator Input Sensitivity			0.2	V_{CC}	V_{PP}
DIGITAL INTERFACE (CE, DATA, CLK, LE, LD)						
V_{IH}	High-Level Input Voltage		0.8 V_{DD}		V_{DD}	V
			0.8 V_{CC}		V_{CC}	V
V_{IL}	Low-Level Input Voltage		0		0.2 V_{DD}	V
			0		0.2 V_{CC}	V
I_{IH}	High-Level Input Current	V_{IH} = V_{DD} = V_{CC}			10	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0V	−10			µA
C_I	Input Capacitance			3.0		pF
V_{OH}	High-Level Output Voltage		0.9 V_{DD}			V
			0.9 V_{CC}			V
V_{OL}	Low-Level Output Voltage				0.1 V_{DD}	V
					0.1 V_{CC}	V
C_O	Output Capacitance				5.0	pF

(4) For frequencies other than the default values, the SPI_DEF bit should be set to 0 and registers R4 and R5 programmed appropriately. Refer to Serial Port Interface Default Register Selection for further details on how to program the SPI_DEF bit.

(5) For other reference oscillator frequencies, please contact Texas Instruments.

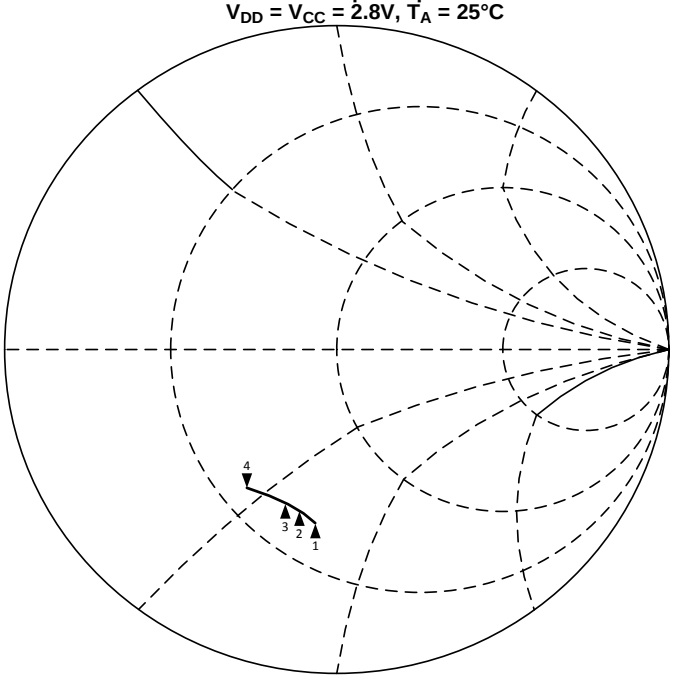
Electrical Characteristics (continued)

V_{CC} = V_{DD} = CE = 2.8V, T_A = +25°C, unless otherwise specified

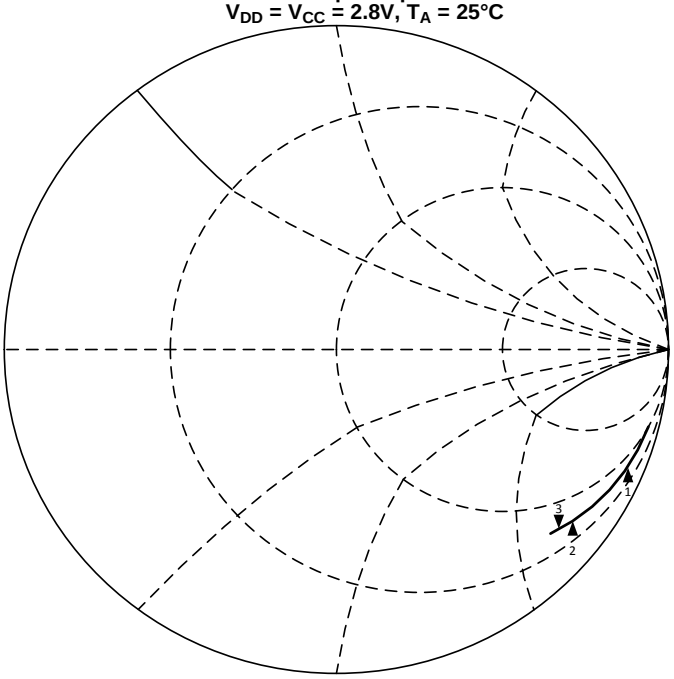
Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
MICROWIRE INTERFACE						
t_{CS}	DATA to CLK Set Up Time		50.0			ns
t_{CH}	DATA to CLK Hold Time		10.0			ns
t_{CWH}	CLK Pulse Width HIGH		50.0			ns
t_{CWL}	CLK Pulse Width LOW		50.0			ns
t_{ES}	CLK to LE Set Up Time		50.0			ns
t_{EW}	LE Pulse Width		50.0			ns

Typical Performance Characteristics

RF VCO Output Impedance
V_{DD} = V_{CC} = 2.8V, T_A = 25°C



IF PLL Input Impedance
V_{DD} = V_{CC} = 2.8V, T_A = 25°C



RFout (MHz)	R Ω	jX Ω	|R + jX| Ω
2087.73	26.406	−34.650	46.564
2105.28	25.385	−30.800	39.913
2121.00	23.898	−28.122	36.905
2155.14	19.979	−23.102	30.543

Fin (MHz)	R Ω	jX Ω	|R + jX| Ω
170.76	33.789	−239.220	241.595
367.20	26.992	−137.620	140.242
440.76	27.844	−126.470	129.499

Serial Data Input Timing

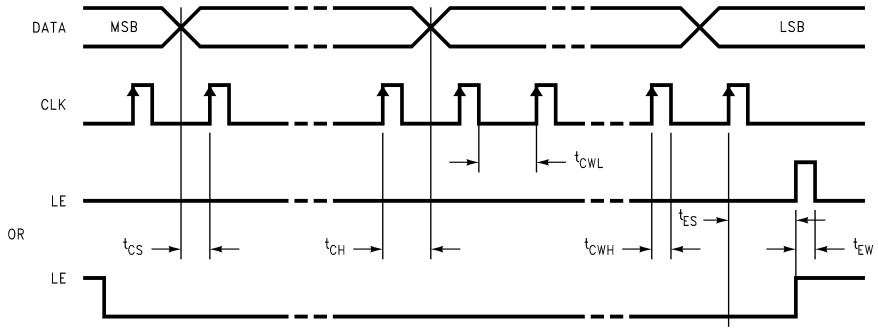


Figure 1. Serial Data Input Timing

NOTE

1. DATA is clocked into the 24-bit shift register on the rising edge of CLK.
2. The MSB of DATA is shifted in first.

FUNCTIONAL DESCRIPTION

LMX2542 is a highly integrated, high performance, low power, frequency synthesizer system optimized for Cellular-CDMA 1xRTT and IS-95 mobile handsets and data systems with GPS capabilities. Using a proprietary digital phase locked loop technique, LMX2542 generates very stable, low noise local oscillator (LO) signals for up and down conversion in wireless communications devices.

LMX2542 includes a Voltage Controlled Oscillator (VCO) for the Cellular-CDMA and GPS frequency bands, a loop filter, and a Fractional-N RF PLL based on a ΔΣ modulator which supports frequency resolutions as low as 5 kHz. In concert, these blocks form a closed loop RF synthesizer system. The RF synthesizer system operates from 2087.73 MHz to 2155.14 MHz. The need for external components is limited to a few passive elements for matching the RF output impedance, and bypass elements for power line stabilization.

The Fractional-N RF PLL (ΔΣ modulator architecture) delivers low spurious thus providing a significant improvement over other PLL solutions. In addition, the Fractional-N RF PLL facilitates faster lock times, which reduces power consumption and system set-up time. Furthermore, the RF loop filter occupies a much smaller area as opposed to the Integer-N architecture. This allows the RF loop filter to be embedded into the circuit, thus minimizing the external noise coupling.

LMX2542 includes an Integer-N IF PLL also. For more flexible loop filter designs, the IF PLL includes a 4-level programmable charge pump. Together with an external VCO and loop filter, LMX2542 makes a complete closed loop IF synthesizer system. The default IF frequency is 367.20 MHz.

The circuit also supports commonly used reference oscillator frequencies of 19.20 MHz and 19.68 MHz.

FREQUENCY GENERATION

RF Frequency Selection

The RF synthesizer (Cellular-CDMA) divide ratio can be calculated using the following equation:

$$f_{RFout} = \left(8 \cdot RF\_B + RF\_A + \frac{10^4 \cdot RF\_FN}{f_{OSCin}}\right) \cdot f_{OSCin}$$

where

- RF_A < RF_B
- f_{RFout} : RF VCO output frequency
- f_{OSCin} : Reference oscillator frequency
- RF_A : Preset divide ratio of the RF PLL binary 3-bit swallow counter (0 ≤ RF_A ≤ 7)
- RF_B : Preset divide ratio of the RF PLL binary 4-bit programmable counter (2 ≤ RF_B ≤ 15)
- RF_FN : Preset numerator of the RF PLL binary 11-bit modulus counter (0 ≤ RF_FN < 1920 for f_{OSCin} = 19.20 MHz) (0 ≤ RF_FN < 1968 for f_{OSCin} = 19.68 MHz) (1)

NOTE

When the FREQ_OFF bit is set to 1, frequencies with 5 kHz resolution can be generated. In the same way outlined above, the divide ratio for the desired frequency less 5 kHz should be programmed. When the FREQ_OFF bit (R1[2]) is set to 1, the programmed frequency will be shifted by +5 kHz in order to achieve the desired frequency. Refer to RF Synthesizer System Frequency Offset for details on how to program the FREQ_OFF bit.

IF Frequency Selection

The IF synthesizer divide ratio can be calculated using the following equation:

$$f_{Fin} = (16 \cdot IF\_B + IF\_A) \cdot \frac{f_{OSCin}}{IF\_R}$$

where

- IF_A < IF_B
- f_{Fin} : IF VCO output frequency
- f_{OSCin} : Reference oscillator frequency
- IF_A : Preset divide ratio of the IF PLL binary 4-bit swallow counter (0 ≤ IF_A ≤ 15)
- IF_B : Preset divide ratio of the IF PLL binary 9-bit programmable counter (1 ≤ IF_B ≤ 511)
- IF_R : Preset divide ratio of the IF PLL binary 9-bit programmable reference counter (2 ≤ IF_R ≤ 511) (2)

From the above equation and with the SPI_DEF bit set to 1, LMX2542 generates a fixed IF frequency of 367.20 MHz as follows:

f_{Fin} (MHz)	IF_B	IF_A	f_{OSCin} / IF_R (kHz)
367.20	191	4	120

VCO FREQUENCY TUNING

The center frequency of the RF VCO is determined mainly by the resonant frequency of the tank circuit. This tank circuit is implemented on-chip and requires no external inductor. LMX2542 actively tunes the tank circuit to the required frequency with the built-in tracking algorithm.

POWER CONTROL

LMX2542 includes a powerdown mode to reduce the power consumption. LMX2542 can be powered down when the CE pin is set LOW, independent of the state of the powerdown bits. When CE is set HIGH, powerdown is controlled through the MICROWIRE. The RF and IF circuitries are individually powered down by setting the RF_EN (R1[3]) and IF_EN (R2[2]) bits LOW respectively. Refer to RF Synthesiser System Enable and IF Synthesizer Enable for details on how to program the RF_EN and IF_EN bits.

CE Pin	RF_EN	IF_EN	RF Circuitry	IF Circuitry
0	X	X	OFF	OFF
1	0	0	OFF	OFF
1	0	1	OFF	ON
1	1	0	ON	OFF
1	1	1	ON	ON

NOTE

1. X refers to a don't care condition.
2. The RF circuitry includes the whole RF synthesizer system (synthesizer and VCO).
3. The IF circuitry includes the IF synthesizer block only.

RF DIGITAL FILTERED LOCK DETECT

A digital filtered lock detect status generated from the RF phase frequency detector (PFD) is available on the LD pin (Pin 19) when the RF_LD bit (R0[21]) is set to 1. The LD output is therefore used to indicate the lock status of the RF synthesizer system. Furthermore, the LD output can be forced to GND at all times when the RF_LD bit is set to 0.

When used as a lock detect output, the two inputs to the PFD, f_N and f_R, are first divided by 64. The lock detect digital filter then compares the difference between the phases of the inputs to the PFD to an RC generated delay of approximately 10 ns. This delay is represented by t_W in Figure 2 and Figure 3 below. If the phase error is less than 10 ns ($\Delta t < t_W$) for 4 consecutive PFD comparison cycles, the RF PLL enters a locked state and the LD output is then forced HIGH. Once the phase error becomes greater than 10 ns ($\Delta t > t_W$) the RF PLL falls out of lock and the LD is forced LOW (~GND). The phase error in Figure 3 is measured on the leading edge. If the phase difference between the two inputs to the PFD is equal to 10 ns ($\Delta t = t_W$), then the LD output becomes unpredictable. Refer to RF Synthesizer Lock Defect for further details on how to program the digital filtered lock detect.

NOTE

f_R is the PFD input from the reference oscillator and f_N is the PFD input from the programmable feedback divider (N counter).

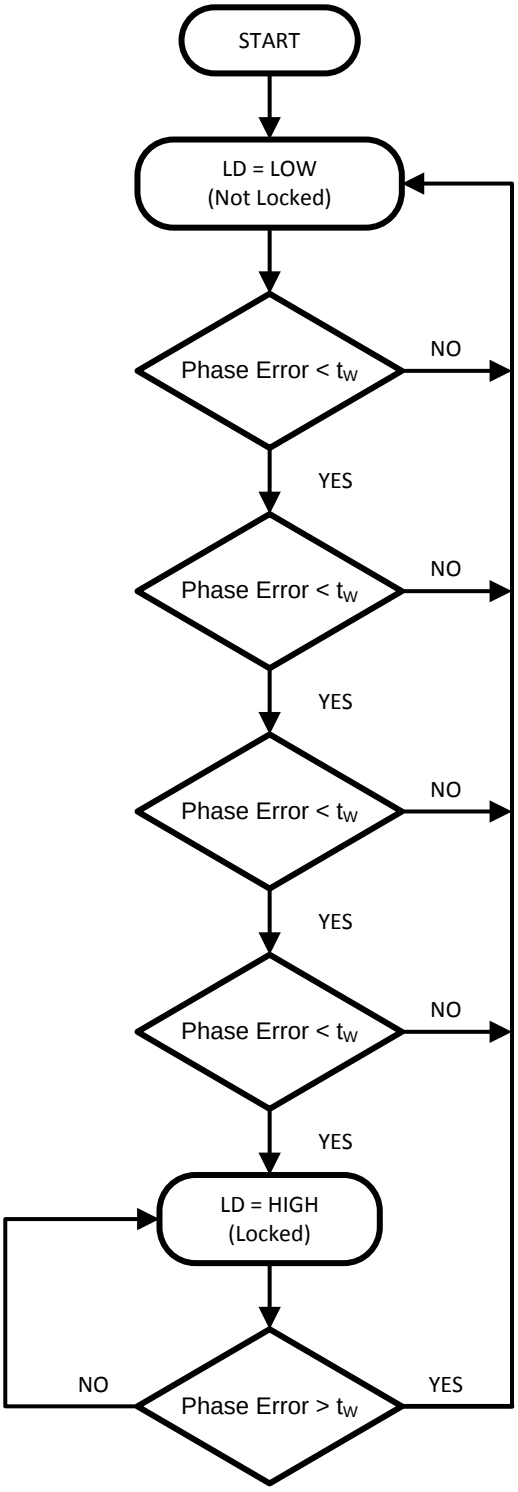


Figure 2. Lock Detect Flow Diagram

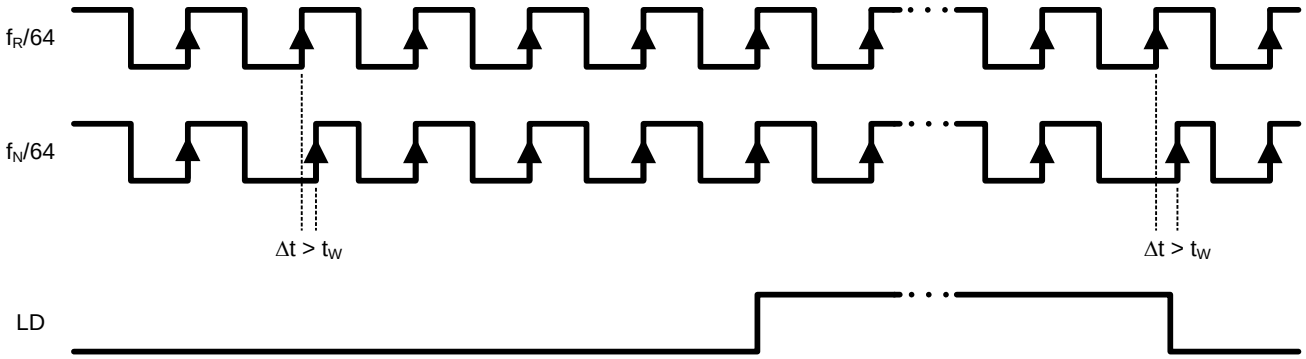


Figure 3. Lock Detect Timing Diagram Waveform

MICROWIRE SERIAL INTERFACE

The programmable register set is accessed via the MICROWIRE serial interface. The interface comprises three signal pins: CLK, DATA, and LE. Serial data is clocked into the 24-bit shift register on the rising edge of CLK. The least significant bits decode the internal control register address. When LE transitions from LOW to HIGH, DATA stored in the shift registers is loaded into one of six control registers. The MSB of DATA is loaded in first. The synthesizers can be programmed even in power down mode. A complete programming description is provided in Programming Description.

Programming Description

MICROWIRE INTERFACE

The MICROWIRE Serial Port Interface (SPI) has a 24-bit shift register to store the incoming DATA bits temporarily. The incoming DATA is loaded into the shift register from MSB to LSB. The data is shifted at the rising edge of the CLK signal. When the LE signal transitions from LOW to HIGH, the DATA stored in the shift register is transferred to the proper register depending on the state of the ADDRESS bits. The selection of the particular register is determined by the address bits equal to the binary representation of the number of the control register.

At start-up, the 24-bit shift register is loaded via the MICROWIRE interface. The loading requires 3 default words, with register R2 loaded first, and R0 loaded last. Once loaded, the RF VCO frequency can then be changed by only programming register R0 appropriately. If an IF frequency other than the default value is desired, the SPI_DEF bit should be set to 0, and registers R4 and R5 programmed appropriately.

Control Register Content Map

The control register content map describes how the bits within each control register are allocated to specific control functions. The bits that are marked 0 should be programmed as such to ensure proper device operation.

Table 1. Control Register Content Map

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB	SHIFT REGISTER BIT LOCATION																						LSB
R0	SPI_DEF	1	RF_LD	0	RF_B [3:0]				RF_A [2:0]			RF_FN [10:0]											**0**	**0**
R1	0	1	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	1	OB_CRL [1:0]		RF_EN	FREQ_OFF	**0**	**1**
R2	1	1	0	0	1	0	0	1	0	0	0	0	0	0	VCO_CUR [1:0]		OSC_FREQ	IF_FREQ [1:0]		IF_CUR [1:0]		IF_EN	**1**	**0**
R3	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	**0**	**1**	**1**
R4	0	0	0	0	0	0	0	IF_A [3:0]				IF_B [8:0]									**0**	**1**	**1**	**1**
R5	0	0	0	0	0	0	0	0	0	0	IF_R [8:0]									**0**	**1**	**1**	**1**	**1**
R6	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	**0**	**1**	**1**	**1**	**1**	**1**

NOTE

Numbers in **Bold** represent the ADDRESS bits.

R0 REGISTER

The R0 register contains the RF_FN, RF_A, RF_B, RF_LD, and SPI_DEF control words. The register address bits are R0[1:0] = 00. The detailed descriptions and programming information for each control word is discussed in the following sections.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	DATA[21:0] FIELD																						ADDRESS [1:0] FIELD	
R0	SPI_DEF	1	RF_LD	0	RF_B [3:0]				RF_A [2:0]			RF_FN [10:0]											**0**	**0**

RF_FN[10:0] - RF Synthesizer Fractional Numerator Counter (R0[2:12])

The RF_FN control word is used to setup the 11-bit ΔΣ modulator. This corresponds to programming the fractional numerator counter portion of the RF feedback divider. The value programmed is dependent on the reference oscillator used.

Programming RF_FN[10:0] Using 19.20 MHz Reference Oscillator

When a 19.20 MHz reference oscillator is used (OSC_FREQ bit = 0), the RF_FN can be programmed to values ranging from 0 to 1919.

Numerator	RF_FN[10:0] f_{OSCin} = 19.20 MHz										
	10	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
1919	1	1	1	0	1	1	1	1	1	1	1

Programming RF_FN[10:0] Using 19.68 MHz Reference Oscillator

Similarly, when a 19.68 MHz reference oscillator is used (OSC_FREQ bit = 1), the RF_FN can be programmed to values ranging from 0 to 1967.

Numerator	RF_FN[10:0] f_{OSCin} = 19.68 MHz										
	10	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
1967	1	1	1	1	0	1	0	1	1	1	1

RF_A[2:0] - RF Synthesizer Swallow Counter (A Counter) (R0[13:15])

The RF_A control word is used to setup the RF synthesizer's A counter. The A counter is a 3-bit swallow counter used in the programmable feedback divider. The RF_A control word can be programmed to values ranging from 0 to 7.

Divide Ratio	RF_A[2:0] RF Mode		
	2	**1**	**0**
0	0	0	0
1	0	0	1
•	•	•	•
7	1	1	1

RF_B[3:0] - RF Synthesizer Programmable Binary Counter (B Counter) (R0[16:19])

The RF_B control word is used to setup the RF synthesizer's B counter. The B counter is a 4-bit programmable binary counter used in the programmable feedback divider. The RF_B control word can be programmed to values ranging from 2 to 15. Divide ratios less than 2 are prohibited.

Divide Ratio	RF_B[3:0]			
	3	**2**	**1**	**0**
2	0	0	1	0
3	0	0	1	1
•	•	•	•	•
15	1	1	1	1

RF_LD - RF Synthesizer System Lock Detect (R0[21])

The RF_LD bit is used to indicate the lock status of the RF synthesizer system.

Control Bit	Register Location	Description	Function	
			0	1
RF_LD	R0[21]	RF Synthesizer System Lock Detect	Hard Zero (GND)	Lock Detect

SPI_DEF - Serial Port Interface Default Register Selection (R0[23])

The SPI_DEF bit selects between using the default IF counter values and user programmable values.

Control Bit	Register Location	Description	Function	
			0	1
SPI_DEF	R0[23]	Serial Port Interface Default Register Selection	Default Counter Values OFF. Program Registers R0 through R6	Default Counter Values ON. Program Registers R0 through R2

R1 REGISTER

The R1 register contains the FREQ_OFF, RF_EN and OB_CRL control words. The register address bits are R1[1:0] = 01. The detailed descriptions and programming information for each control word is discussed in the following sections.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	DATA[21:0]																						ADDRESS [1:0] FIELD	
R1	0	1	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0	1	OB_CRL [1:0]		RF_EN	FREQ_OFF	**0**	**1**

FREQ_OFF - RF Synthesizer System Frequency Offset (R1[2])

The FREQ_OFF bit is used to offset the RF frequency by +5 kHz.

Control Bit	Register Location	Description	Function	
			0	1
FREQ_OFF	R1[2]	RF Synthesizer System Frequency Offset	RF Synthesizer System Frequency Offset Disabled	RF Synthesizer System Frequency Offset Enabled

RF_EN - RF Synthesizer System Enable (R1[3])

The RF_EN bit is used to switch the RF synthesizer system (PLL and VCO) between a powered up and powered down mode.

Control Bit	Register Location	Description	Function	
			0	1
RF_EN	R1[3]	RF Synthesizer System Enable	RF Synthesizer System Powered Down	RF Synthesizer System Active

OB_CRL[1:0] - RF VCO Output Buffer Power Control (R1[5:4])

The OB_CRL word is used to set the RF VCO output buffer power level. The power level can be set according to the system requirements.

OB_CRL[1:0]		RF VCO Output Buffer Power Level (dBm)
0	0	−4.5
0	1	−2.0
1	0	0.5
1	1	3.0

R2 REGISTER

The R2 register contains the IF_EN, IF_CUR, IF_FREQ, OSC_FREQ, and VCO_CUR control words. The register address bits are R2[1:0] = 10. The detailed descriptions and programming information for each control word is discussed in the following sections.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	DATA[21:0] FIELD																						ADDRESS [1:0] FIELD	

R2	1	1	0	0	1	0	0	1	0	0	0	0	0	0	VCO_CUR [1:0]	OSC_FREQ	IF_FREQ [1:0]	IF_CUR [1:0]	IF_EN	**1**	**0**

IF_EN - IF Synthesizer Enable (R2[2])

The IF_EN bit is used to switch the IF synthesizer between a powered up and powered down mode.

Control Bit	Register Location	Description	Function	
			0	1
IF_EN	R2[2]	IF Synthesizer Enable	IF Synthesizer Powered Down	IF Synthesizer Active

IF_CUR[1:0] - IF Synthesizer Charge Pump Current Gain (R2[4:3])

The IF_CUR control word is used to set the IF synthesizer's charge pump current gain. Four gain levels are available.

IF_CUR[1:0]		IF Synthesizer Charge Pump Current Gain (µA)
0	0	100
0	1	200
1	0	300
1	1	800

IF_FREQ[1:0] - IF Synthesizer Fixed Frequency Selection (R2[6:5])

The IF_FREQ control word is used to set the default fixed IF frequency applicable to the specific CDMA system. For LMX2542, the default fixed IF frequency is 367.20 MHz.

IF_FREQ[1:0]		Fixed IF Frequency (MHz)
0	0	170.76
0	1	367.20
1	0	440.76

OSC_FREQ - Reference Oscillator Frequency Select (R2[7])

The OSC_FREQ bit is used to select the appropriate reference oscillator frequency.

Control Bit	Register Location	Description	Function	
			0	1
OSC_FREQ	R2[7]	Reference Oscillator Select	19.20 MHz Reference Oscillator Selected	19.68 MHz Reference Oscillator Selected

VCO_CUR[1:0] - RF VCO Dynamic Current (R2[9:8])

The VCO_CUR control word is used to set the dynamic current for the RF VCO. A maximum dynamic current is recommended, and is achieved when VCO_CUR[1:0] word = 11.

VCO_CUR[1:0]		RF VCO Current Magnitude
0	0	Minimum
•	•	•
•	•	•
1	1	Maximum

R3 REGISTER

The R3 register is used for internal testing of the device and is not intended for customer use. The register address bits are R3[2:0] = 011. Register R3 is active only when the SPI_DEF bit in Register R0 is set to 0.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	DATA[20:0] FIELD																					ADDRESS [2:0] FIELD		
R3	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	**0**	**1**	**1**

R4 REGISTER

The R4 register contains the IF_B and IF_A control words. The register address bits are R4[3:0] = 0111. Register R4 is active only when the SPI_DEF bit in Register R0 is set to 0. Regsiter R4 should only be used to set the IF N counter if the default value is not desired. The detailed descriptions and programming information for each control word is discussed in the following sections.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	DATA[19:0]																				ADDRESS [3:0] FIELD			
R4	0	0	0	0	0	0	0	IF_A [3:0]				IF_B [8:0]									**0**	**1**	**1**	**1**

IF_B[8:0] - IF Synthesizer Programmable Binary Counter (B Counter) (R4[12:4])

The IF_B control word is used to setup the IF synthesizer's B counter. The B counter is a 9-bit programmable binary counter used in the programmable feedback divider. The IF_B control word can be programmed to values ranging from 1 to 511. Divide ratios less than 1 are prohibited.

Divide Ratio	IF_B[8:0]								
	8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	1	0
•	•	•	•	•	•	•	•	•	•
511	1	1	1	1	1	1	1	1	1

IF_A[3:0] - IF Synthesizer Swallow Counter (A Counter) (R4[16:13])

The IF_A control word is used to setup the IF synthesizer's A counter. The A counter is a 4-bit swallow counter used in the programmable feedback divider. The IF_A control word can be programmed to values ranging from 0 to 15.

Divide Ratio	IF_A[3:0]			
	3	**2**	**1**	**0**
0	0	0	0	0
1	0	0	0	1
•	•	•	•	•
15	1	1	1	1

R5 REGISTER

The R5 register contains the IF_R control word. The register address bits are R5[4:0] = 01111. Register R5 is active only when the SPI_DEF bit in Register R0 is set to 0. Regsiter R5 should only be used to set the IF R counter if the default value is not desired. The detailed description and programming information for this control word is discussed in the following section.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	DATA[18:0] FIELD																			ADDRESS [4:0] FIELD				
R5	0	0	0	0	0	0	0	0	0	0	IF_R [8:0]									**0**	**1**	**1**	**1**	**1**

IF_R[8:0] - IF Synthesizer Programmable Reference Divider (R5[13:5])

The IF_R control word is used to setup the IF synthesizer's reference divider. The IF_R control word can be programmed to values ranging from 2 to 511. Divide ratios less than 2 are prohibited.

Divide Ratio	IF_R[8:0]								
	8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
2	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•
511	1	1	1	1	1	1	1	1	1

R6 REGISTER

The R6 register is used for internal testing of the device and is not intended for customer use. The register address bits are R6[5:0] = 011111. Register R6 is active only when the SPI_DEF bit in Register R0 is set to 0.

Reg	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	DATA[17:0] FIELD																		ADDRESS [5:0] FIELD					
R6	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	**0**	**1**	**1**	**1**	**1**	**1**

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	23

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